

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Hussein I. Hanafi, et al.

Examiner: Stanetta D. Isaac

Serial No.: 10/639,942

Art Unit: 2812

Filed: August 13, 2003

Docket: YOR920020257US1 (15949)

Dated: February 14, 2005

For: DEVICE THRESHOLD VOLTAGE CONTROL OF FRONT-GATE SILICON-ON-INSULATOR MOSFET USING A SELF-ALIGNED BACK-GATE

Confirmation No. 6974

Mail stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R §§1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. U.S. Patent Application No. US 6,580,132 B1, issued June 17, 2003, issued to Chan, et al.; and
2. U.S. Patent Application No. US 6,528,376 B1, issued March 4, 2003, issued to Guo Jyh-Chyurn; and

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date set forth below.

Dated: February 14, 2005



Leslie S. Szivos, Ph.D.

3. U.S. Patent Application No. US 6,339,002 B1, January 15, 2002, issued to Chan, et al.; and

4. U.S. Patent Application No. US 5,773,331 A, issued June 30, 1998, issued to Wong Hon-Sum Philip, et al.; and

5. U.S. Patent Application No. US 5,346,839 A, issued September 13, 1994, issued to Sundaresan Ravishankar ; and

6. International Patent Publication No. WO 02/101811 A, issued December 19, 2002; and

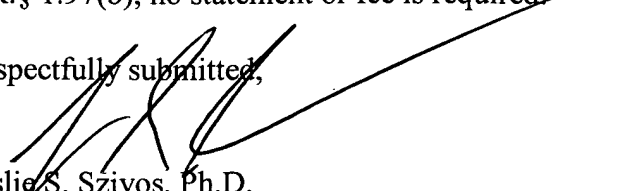
7. Guarini K W, et al., "Triple-self aligned, planar double-gate MOSFETs: devices and circuits" International Electron Devices Meeting 2001. IEDM. Technical Digest. Washington, DC, Dec. 2-5, 2001, New York, NY: IEEE, US, 2 December 2001 (2001-12-02), pp 1921-1924.

The references were cited in a Search Report dated February 2, 2005 received from the European Patent Office. Applicant is submitting copies of the above-cited references, together with a copy of the Search Report. The relevance of the above-identified references has been described in the Search Report.

In accordance with the waiver of 37 C.F.R. § 1.98 (a)(2)(i), per 1276 OG 55, August 5, 2003, applicants are not required to submit copies of the above-cited U.S. Patent references. Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

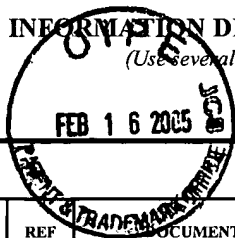
Respectfully submitted,



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INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)



| | | |
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| Docket Number (Optional) YOR920020257US1 (15949) | | Application Number 10/639,942 |
| Applicant(s) Hussein I. Hanafi, et al. | | |
| Filing Date August 13, 2003 | Group Art Unit 2812 | |

U.S. PATENT DOCUMENTS

| *EXAMINER INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|----------------------|-----|-----------------|----------|-----------------------------|-------|----------|-------------------------------|
| | | 6,580,132 B1 | 06/17/03 | Chan, et al. | | | |
| | | 6,528,376 B1 | 03/04/03 | Guo Jyh-Chyurn | | | |
| | | 6,339,002 B1 | 01/15/02 | Chan, et al. | | | |
| | | 5,773,331 A | 06/30/98 | Wong Hon-Sum Philip, et al. | | | |
| | | 5,346,839 A | 09/13/94 | Sundaresan Ravishankar | | | |

U.S. PATENT APPLICATION PUBLICATIONS

| *EXAMINER INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
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FOREIGN PATENT DOCUMENTS

| | REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|--|-----|-----------------|----------|---------|-------|----------|-------------|----|
| | | | | | | | YES | NO |
| | | WO 02/101811 A | 19-12-02 | PCT | | | | |
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| | | Guarini K W, et al., "Triple-self aligned, planar double-gate MOSFETs: devices and circuits" International Electron Devices Meeting 2001. IEDM. Technical Digest. Washington, DC, Dec. 2-5, 2001, New York, NY: IEEE, US, 2 December 2001 (2001-12-02), pp 1921-1924. |
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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.